VERIFICATION OF SYSTEM ARCHITECTURES USING MODAL LOGICS AND FORMAL MODEL CHECKING TECHNIQUES*

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ABSTRACT

An application of formal model checking techniques for developing analysis and assessment mechanisms for system architectures developed in accordance with the DoD Architecture Framework (DoDAF) is presented. The use of temporal logics for capturing a system’s correctness requirements and the use of an architecture design process to refine these specifications are proposed. A computer-aided verification approach is described that employs the executable model, derived from the framework products, and the formal logic statements to establish correctness of the developed system architecture. The approach is presented with the help of an illustrative example.